



(11) Publication number : **0 558 291 A2**

(12)

## EUROPEAN PATENT APPLICATION

(21) Application number : **93301358.3**

(51) Int. Cl.<sup>5</sup> : **H04Q 11/04**

(22) Date of filing : **24.02.93**

(30) Priority : **26.02.92 GB 9204100**

(43) Date of publication of application :  
**01.09.93 Bulletin 93/35**

(84) Designated Contracting States :  
**DE ES FR IT SE**

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(54) **Reconfigurable switch memory.**

(57) A reconfigurable switch memory which is applicable to time switches and space switches enables two very different time switching functions to be efficiently implemented by one type of switching unit. A reconfigurable switching device is provided which, for instance, can work in either one bit or five bit mode, the granularity of the switch being varied.

Fig.7.

INTERFACES	UNITS PER PLANE	AVAILABLE GRANULARITIES						
		VC 4	VC 3	VC 2	VC 12	VC 11	NX64 kb/s	64 kb/s
STM-1 (64kb/s)								
4 (9K)	1 CARD	*	*	*	*	*	*	*
8 (19K)	1 CARD	*	*	*	*	*	*	*
16 (38K)	2 CARDS	*	*	*	*	*	*	*
32 (77K)	1 UNIT	*	*	*	*	*	*	*
64 (155K)	2 UNITS	*	*	*	*	*	*	*
160	5 UNITS + B/SPREAD	*	*	*	*	*	*	*
320	10 UNITS + B/SPREAD	*	*	*	*	*	*	*

The technique described is applicable to time switches and space switches. The time switching function will be the one described in more detail.

It enables two very different time switching functions to be efficiently implemented by one type of switching unit.

5 There are many designs of, for instance, 64 kbit/s time switches, normally having a common frame structure.

They normally have a speech store, to hold the data samples and a control store, to define which data sample is to be routed to a particular time slot on a particular output port.

The 64 kbit/s frame structure has timeslots of 8 bits. The Frame repetition rate is 125 microseconds.

10 Internal to the switch, it is not uncommon to carry some extra signalling or check bits and the switch may therefore carry perhaps 10 bits instead of 8 bits.

There are newer transmission formats which are still based on a Frame structure of 125 microseconds, but which are divided, in time, into 9 rows. Consequently the switch has to handle 9 timeslots per frame for each channel. It therefore has to handle a timeslot every ninth of a Frame. All the nine timeslots are routed to the same destination. It is therefore possible to use a time switching device which contains a data sample store and a control store which have only one ninth of the locations of a normal 64 kbit/s switch. This type of switch is often referred to as a Column switch.

15 A time switching device which has to operate on a fixed number of input and output ports of a fixed data rate, may be required to perform both 64 kbit/s switching and Column switching. When it is operating as a Column switch it is not using the memory efficiently.

It is known that in order to limit the amount of bandwidth carried by one time switching device, it is possible to have several switches in parallel where each device only handles one or some of the bits of a time slot. This technique is referred to as bit spreading.

This technique results in a copy of the control store being required in each of the parallel switching devices.

25 This technique also results in a larger number of channels being handled by the device and consequently a higher number of speech store accesses. This in turn can result in multiple copies of the speech stores because of the limited access times of the storage devices used.

Bit spreading makes the building of very large switches easier, but requires much more storage to do it.

30 So far only two features have been mentioned. Firstly, that a Column switch only needs one ninth of the memory of a directly equivalent 64 kbit/s switch and secondly, that bit spreading uses more memory.

It is possible to combine a 64 kbit/s switching function and a bit spreading column switching function, where the total storage requirements are within a factor of 2 of each other.

35 The 64 kbit/s function internally is a 10 bit timeslot. This is split into two 5 bit half timeslots for the full size switch. The Column function is also based on 10 bit timeslots, which are carried as individual bits for the full size switch.

The full size Column switch has ten switch arrays each carrying one bit.

A half size Column switch has five switch arrays each carrying two bits.

A fifth size Column switch has two switch arrays each carrying five bits, which is the same arrangement as the full size 64 kbit/s switch.

40 A tenth size Column switch has one switch array each carrying 10 bits, which is the same arrangement as the half size 64 kbit/s switch.

This switching device is reconfigurable so that it can work in either one bit or 5 bit mode. This results in common high capacity 64 kbit/s and Column switching functions realised from a common time switching device.

45 Large switches are often made up of a combination of space switching and time switching devices. Space switching devices can also have their control stores reconfigured in the same manner.

According to the present invention there is provided a Synchronous Transfer Mode (STM) switching unit wherein the granularity of the switch may be varied.

The present invention will now be described, by way of example, with reference to the accompanying drawings, in which :

50 Figures 1(a) - 1(g) show examples of a range of STM-1 switches;

Figures 2(a) - 2(g) show examples of switching unit structure corresponding to Figures 1(a) - 1(g);

Figure 3 shows a diagrammatic view of an orthogonal switching unit;

Figures 4(a) - 4(e) show examples of single stage switch capacities;

Figures 5(a) - 5(c) show examples of switching elements;

55 Figures 6(a) and 6(b) show examples of time switch ASICs;

Figure 7 shows a table of switch growth states.

A good telecommunications switch needs more than just sound switching theory. It needs to meet its functional requirements and it also needs to be a soundly engineered product.

There are many switching theory techniques, a number of ways of functionally partitioning such techniques, and even more implementation methods.

A switch has to be able to transfer input circuits to output circuits, a multipurpose switch has to be able to handle more than one type of circuit.

There are two simple measures of switch capacity:

interface bandwidth capacity; which is the sum of the bandwidths of all the interfaces,

and circuit capacity; which is the total number of circuits the switch fabric can switch.

For a particular interface bandwidth capacity, as the granularity of the switch reduces the circuit capacity increases. As the circuit capacity increases the memory requirements of the switching elements increase as does the complexity of the control mechanisms.

Over a range of interface bandwidth capacities and a range of switching granularities the switching memory requirements and the complexity of the control can vary very considerably.

It is apparent that if the switching granularity could increase as the interface bandwidth increases then the circuit capacity would remain constant as would the control complexity.

The amount of memory used is not just a function of interface bandwidth capacity and the circuit capacity. It is also dependent on the basic switch architecture as well as being dependent on the cycle time of the Memory and whether bit spreading is used.

Depending on the architecture and partitioning chosen, switches of the same interface bandwidth capacity can have very different amounts of internal cabling. For example, if the CLOS fanout interconnect is implemented using a backplane rather than cables then, the total internal cables may be halved.

The growth mechanisms can also have dramatic effects on the amount of cabling, if they are not well thought out.

Rather than adding cards to partially empty shelves, a simple way of offering growth is to use more switching units. Building them into arrays has multi-stage and cabling difficulties, but running them in parallel can be quite straight forward. The variable bit spreading method offers very convenient growth characteristics.

For a range of switches, from 32 STM-1 interfaces of 155.52 Mbit/s, up to 320 STM-1 interfaces, 4 configurations can be used.

1 Switch Unit for 32 STM-1 interfaces

2 Switch Units for 64 STM-1 interfaces

5 Switch Units for 160 STM-1 interfaces

10 Switch Units for 320 STM-1 interfaces

Figure 1 gives some examples

1(a)	32 STM-1s	1 Switch Unit	155520 channels of 32 kbit/s
1(b)	32 STM-1s	1 Switch Unit	77760 channels of 64 kbit/s
1(c)	32 STM-1s	1 Switch Unit	8640 columns for VC switching
1(d)	64 STM-1s	2 Switch Units	155520 channels of 64 kbit/s
1(e)	64 STM-1s	2 Switch Units	17280 columns for VC switching
1(f)	128 STM-1s	5 Switch Units	43200 columns for VC switching
1(g)	320 STM-1s	10 Switch Units	86400 columns for VC switching

Bit Spreading units are only required for the two largest switches.

The same switch unit is used for all the above 7 arrangements. It has to operate in 6 different modes to achieve the required switching granularity. The same mode is used for both the 1(a) and 1(d) arrangement.

Figure 2(a) to 2(g) gives the 6 arrangements, of the Space-Time-Spacing switching structure that are used. It receives 64 cables of 116.64 Mbit/s carrying the odd or even bits of an STM-1, or individual bit numbers of 5 different STM-1s. Consequently a single switching unit can handle the equivalent of 32 STM-1s.

All the switching IC inputs and outputs run at a data rate of 19.44 Mbit/s, while the connections through the backplane are at 116.64 Mbit/s.

There are 3 timing options which affect the number and size of the channels handled by both the Time switch elements and the Space switch elements. There are also 2 size options for the space switches.

The time switch elements and time multiplexed space switch elements can operate with;

486 channels of 5 bits over a switching frame of 125  $\mu$ s

or

45 channels of 5 bits over a switching frame of 13.9  $\mu$ s

or

270 channels of 1 bit over a switching frame of 13.9  $\mu$ s 13.9 is one ninth of 125  $\mu$ s and corresponds to an SDH row, as described earlier.

Because the time switching element has 8 inputs and 8 outputs it handles 8 times these numbers of chan-

nels namely, 3888, 432 and 2160 channels for the above 3 arrangements.

The space switch elements supply the CLOS fanout and are either;  
40 x 80 and 80 x 40 or dual 20 x 40 and 40 x 20

The Figure 2(a) to 2(g) arrangement options are as follows;

2(a) & 2(d)	40 x 80	3888 x 5 bits over	125 $\mu$ s	80 x 40
2(b)	dual 20 x 40	3888 x 5 bits over	125 $\mu$ s	dual 40 x 20
2(c)	dual 20 x 40	432 x 5 bits over	13.9 $\mu$ s	dual 40 x 20
2(e)	40 x 80	432 x 5 bits over	13.9 $\mu$ s	80 x 40
2(f)	dual 20 x 40	2160 x 1 bit over	13.9 $\mu$ s	dual 40 x 20
2(g)	40 x 80	2160 x 1 bit over	13.9 $\mu$ s	80 x 40

In order to allow for growth over the range, arrangements 2(c), 2(e), 2(f) and 2(g) do not offer 64 kbit/s switching. Therefore path set ups are performed with a granularity of a column and a switching frame of a row. Whereas for arrangements 2(b) and 2(d), path set ups are performed with a granularity of 64 kbit/s. Arrangements 2(b) and 2(d) can perform VC switching, so 64 kbit/s and VC switching can be performed on the same switch, up to a maximum of 64 STM-1 or equivalent interfaces.

Arrangement 2(a) uses the same configuration of the switching unit as 2(d), but with only one of the switching units.

A Switching Unit contains a 3 stage Space-Time-Space function. There are 8 Outer Space Switching cards. Each Outer Space Switch card carries one first stage space switching element and one third stage space switching element. There are also 8 Central Time Switching cards. Each Central Time Switching card carries 10 second stage time switching elements.

Because of the natural interconnection of a 3 stage switch, it is practicable to use an orthogonal structure, as shown in Figure 3, which makes the handling of the bandwidth within the switching unit much easier. This enables all the CLOS connections to pass directly from one switching stage to the next without the need for any high data rate backplane tracking. It also keeps all these high speed connections quite short.

Single Stage Switches make use of the same Time Switching Element. The space switch element is not used at all.

Only 5 of the similar 3 stage arrangements are listed below and shown in Figures 4(a), 4(b), 4(d), 4(f) and 4(g), (c) and (e) being too small.

4(a) 3888 channels 1 Element 3888 x 5 bits over 125  $\mu$ s for 32 kbit/s

4(b) 1944 channels 1 Element 3888 x 5 bits over 125  $\mu$ s for 64 kbit/s

4(d) 3888 channels 2 Elements 3888 x 5 bits over 125  $\mu$ s for 64 kbit/s

4(f) 4 STM-1s 5 Elements 2160 x 1 bit over 13.9  $\mu$ s for VCs

4(g) 8 STM-1s 10 Elements 2160 x 1 bit over 13.9  $\mu$ s for VCs

Bit spreading occurs on these small VC switches as byte wide data is naturally bit spread.

It should be noted that, the arrangement in Figure 4(g) contains exactly the same switching function i.e. 10 time switching elements, as the Central Time Switching card shown in Figure 3.

Although a switching element is a functional part of the switching architecture, there is no necessity that a switching element is a single integrated circuit.

The architecture is such that the switching elements can be built from Application Specific Integrated Circuits (ASICs) which are of a reasonable size, without large numbers of outputs, without high speed I/Os, without large packages, and without high power dissipation.

All the input and output data rates of the switching elements are 19.44 Mbit/s. This is also true for the ASICs used to implement the elements.

The time-multiplexed space switch ASIC has 40 input switching inputs and 10 outputs. 8 such ASICs can be configured as a 40 x 80 space switch element as shown in Figure 5(a). 8 such ASICs can also be configured as an 80 x 40 space switch element, as shown in Figure 5(b).

The time switch ASIC has 8 switching inputs and 4 switching outputs. 2 of these ASICs are required to make an 8 x 8 time switching element, as shown in Figure 5(c).

Both the Space Switch ASIC and the Time Switch have to be able to work with 486, 54 or 270 channels per output. Therefore the control stores need to each have a maximum capacity of 486 locations.

In a 40 x 10 Time Multiplexed Space Switching ASIC for each output, the Space Switching ASIC has a 40 to 1 multiplexer and a Control Store. There is also a single serial control interface function.

There are 10 Multiplexors and 10 Control Store RAMs.

Each Location of the control store contains 6 bits. 6 bits is sufficient to define which of the 40 inputs is required with some spare values to define what to output when no input is selected. This is essential for idle and diagnostic patterns.

As already explained the control store needs 486 locations. Therefore the total control store RAM of the 40 x 10 Space Switching ASIC requires 29160 bits.

In an 8 x 4 Time Switching ASIC, the ASIC contains; Control Store RAMs, Serial In/parallel Out Registers, a Barrel Shifter, Speech (traffic) Store RAMs and one serial control interface function.

Figure 6(a) shows the general arrangement of the switching ASIC for 5 bit switching and Figure 6(b) for 1 bit switching.

A control store is also needed for each output of the Time Switching ASIC and each needs 486 locations. Because there are a maximum of 3888 channels entering the ASIC, at least 12 bits are needed to select an input channel. 13 bits are provided to supply enough spare values to define what to output when no input is selected. The 4 control store RAMs therefore need to each be 486 x 13, giving a total of 25272 bits.

When the 8 inputs to the ASIC are in 5 bit serial format, 8 Serial In/Parallel Out Registers are required to convert each input to 5 bit parallel format. A 5 to 4 Barrel Shifter is required to give the 4 serial outputs.

Column sequence, byte sequence and bit sequence integrity must be maintained. In order to avoid Double (or Swing) buffering, which increases the delay and memory requirements, the control store does not contain an absolute address of a speech store location. When a speech store access is to be made, the control store is still read. However, it indicates how many memory write cycles have occurred since the require input data was written into the speech store. As the last location written to the speech store is known, the required speech store address can be computed.

Using this technique, as described in our copending Application No. 9105922.0, the depth of the speech store only needs to correspond to the maximum duration for which any data needs to reside in the speech store.

For 64 kbit/s switching the 486 channels per frame has been increased to a maximum memory occupation of 512 write cycles. For VC switching where switching any column to any column is not required, although the maximum memory occupation could be reduced to less than 200 columns, it is convenient to use a value of 256.

In a Speech Store Configuration 5 bit mode, the Speech Store memory requirement, when considering the 64 kbit/s switching needs, has to be able to handle 4096 channels of 5 bits. 4096 channels is 512 x 8, as opposed to 486 x 8 which is 3888.

With 5 bit serial interfaces, 5 clock cycles are available to perform the 8 writes and 4 reads that are necessary for an 8 x 4 Time switch. The Memory therefore has to be organised so that the 8 writes can be performed in parallel during one clock cycle, leaving the other 4 clocks for the 4 random read accesses. This could be 8 RAM blocks of 512 x 5, or one block of 512 x 40. The actual arrangement chosen is 8 RAM blocks of 128 by 20, with a 32:1 selector implemented in two major stages. The multiplexors used also contain further circuitry for injecting idle and test patterns under direction from the control store, although the connections for these are not shown in the Figures.

In a Speech Store Configuration 1 bit mode, for the bit switching mode, in order to hold a complete copy of all the 256 input channels from 8 inputs, 2048 bits are required. Unfortunately for a 256 x 8 RAM, as all the clock cycles would be used for writes, no reads would be possible with single port RAM.

By writing two successive 8 bit input groups into a RAM (128 x 15) at the same time, then some 50% of the clock cycles are free for read accesses. Two such RAMs used alternately provide for a single output switch.

For 4 outputs 4 times the RAM is needed, namely, 8 RAM blocks of 128 x 16. Of course 128 x 20 blocks can be used instead.

Therefore 8 blocks of 128 x 20 bits can be used for the single bit switching mode over one 13.9  $\mu$ s row, as well as for the 5 bit switching mode over a 125  $\mu$ s frame.

Not only are the speech stores built from the same RAMs, but the control stores are also common as are the counters and some of the output multiplexors. Normally changing granularity of a switch has dramatic effect on the quantity of memory used. Using a combination of techniques, limiting the total number of channels, changing the length of the switching frame and using a bit spread architecture for the larger switches enables the same switching ASICs to efficiently meet two very different sets of requirements.

The table shown in Figure 7 lists possible growth states. It also defines the minimum granularity that can be handled by each growth state and indicates the quantity of switching hardware per security plane.

In order to explain the theory, a switching format is assumed which has 9 bits in a byte and 9 rows in frame.

The example is for a single stage time switch.

Switch Format 1

Full length switching frame

One byte switched per channel per frame  
 One switching element per switching function  
 Each switching element switches all  
 nine bits of each byte  
 Each switching element has :-  
 I inputs  
 C channels per input  
 9 bits per channel

Total switch capacity:-  
 $I \times C$  channels of 9 bits per frame  
 Maximum switching delay is 1 frame  
 Ninth length switching frame  
 i.e. one row

Nine bytes switched per channel per frame  
 i.e. One byte switched per channel per row  
 Nine switching elements per switching function  
 Each switching element switches one bit of  
 each byte  
 Each switching element has:-  
 I inputs  
 C channels per input  
 I per bit channel

Total switch capacity:-  
 $I \times C$  channels of 81 bits per frame  
 Maximum switching delay is one ninth frame (1 row)

Switch Format 2 carries 9 times the bandwidth of Switch Format 1.

Comparing switching elements.

The number of inputs is the same (I) (Also equal to the number of inputs).

The number of input channels is the same (C) (Also equal to the number of output channels).

The data rate per input is the same ( $C \times 9$  bits per Frame).

The size of the control store is the same:-

Locations, one per output channel, ( $I \times C$ )

Bits per location is n

(where 2 to the power n is greater than  $I \times C$ )

The size of the speech/traffic store control:-

Minimum number of Locations;

one per input channel ( $I \times C$ )

Bits per location;

Switch Format 1 9 bits

Switch Format 2 1 bit

Read Access Rate;

Switch Format 1 every 9 bits

Switch Format 2 every bit

In the case where the access rate is a critical feature of switching element design, and it normally is when building large circuit switches, then multiple copies of the speech/traffic stores have to be provided for Switch Format 2 type functions.

9 copies of the speech/traffic store are needed for Switch Format 2.

Therefore the Total Memory Requirement for the Speech/traffic store is;

Switch Format 1  $I \times C \times 9$  bits

Switch Format 2  $I \times C \times 9$  bits

The organisation of the memory is different for Switch Formats 1 and 2 but provided it is constructed of several suitable blocks it can be used for either Switch function. When the number of Inputs (I) also equals 9 then it becomes quite straight forward with the addition of suitable multiplexors.

This example which uses a factor of 9 shows that;

A Re-configurable Timing switching element can be used;

(i) Single to make a switch,

or

(ii) By using nine such elements to produce a switch carrying the same number of channels each of 9 times the bandwidth and with a ninth of the switching delay.

The principle applies for any value not just 9.

It applies for space switching elements not just time switches.

It applies for arrays of switches, e.g. SSS STS TST TTT.

It can be also partially applied e.g. 5 bits/1 bit: 5 times size switch: yet 9 to 1 row to frame relationship with some memory inefficiency.

## Claims

1. A Synchronous Transfer Mode (STM) switching unit wherein the granularity of the switch may be varied.
2. An STM switching unit as claimed in Claim 1, having means for a plurality of STM-1 interfaces and being further arranged for 32 kbit/s, 64 bit/s or VC switching.
3. An STM switching unit as claimed in Claim 1 or 2 configured as a time switch.
4. An STM switching unit as claimed in Claim 1 or 2 configured as a space-time-space switch.
5. An STM switching unit as claimed in any preceding claim.

Fig.1(a).

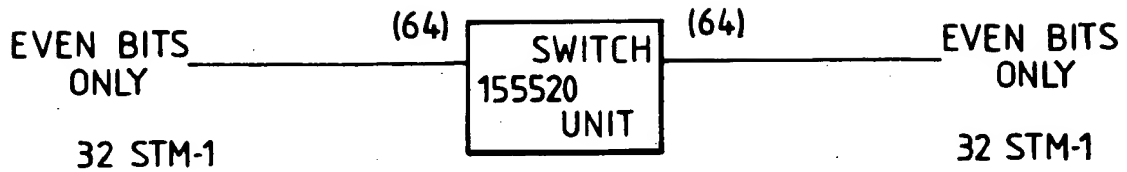


Fig.1(b).

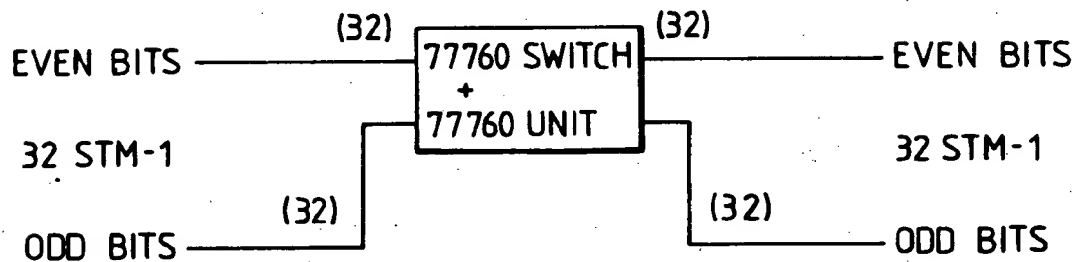


Fig.1(c).

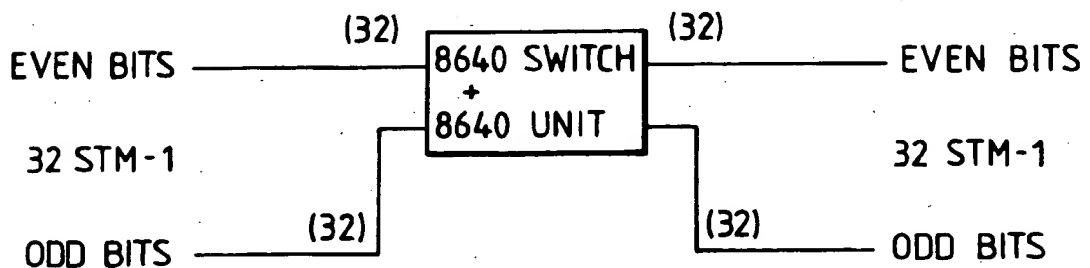




Fig.1(d).

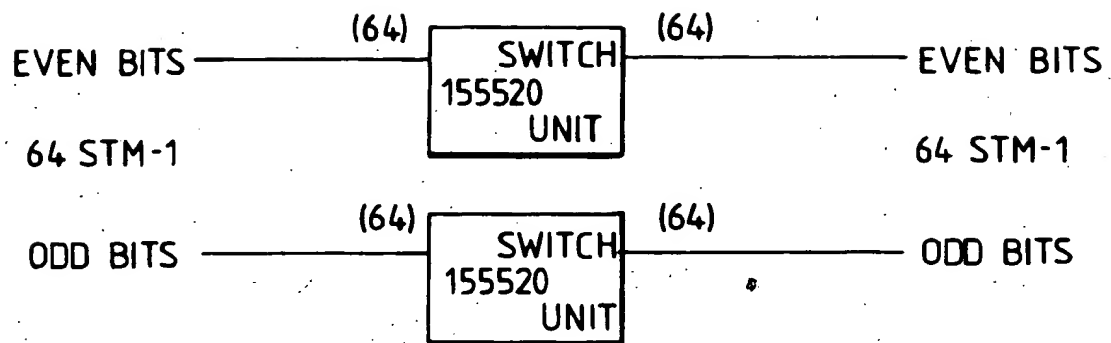


Fig.1(e)

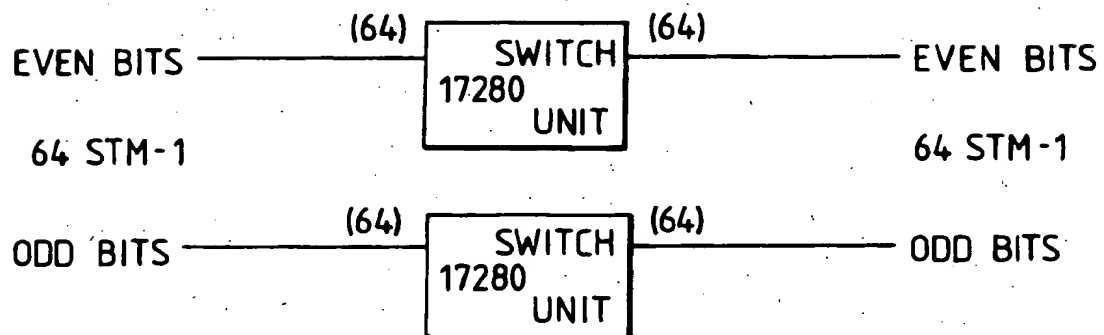


Fig.1(f).

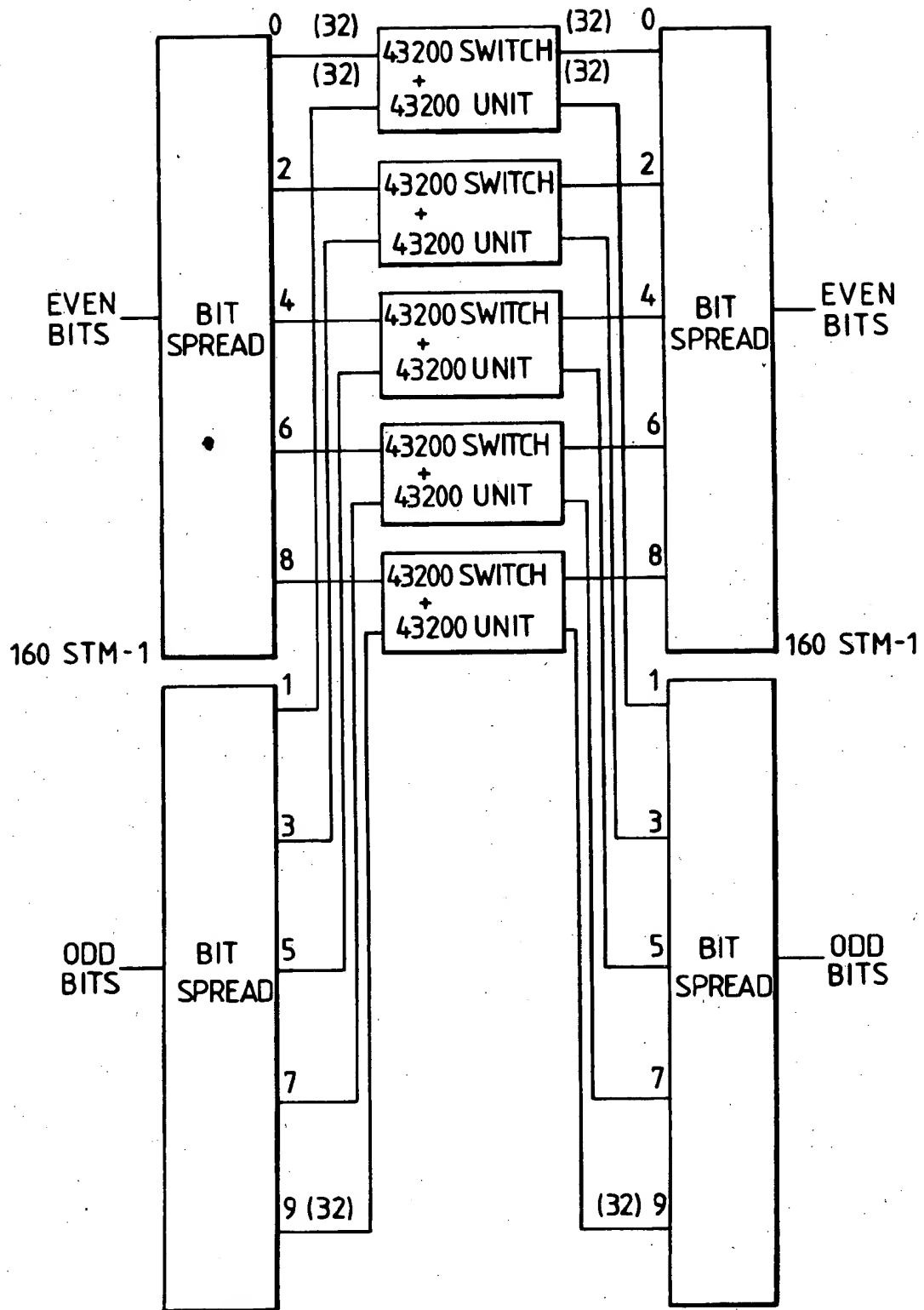


Fig.1 (g).

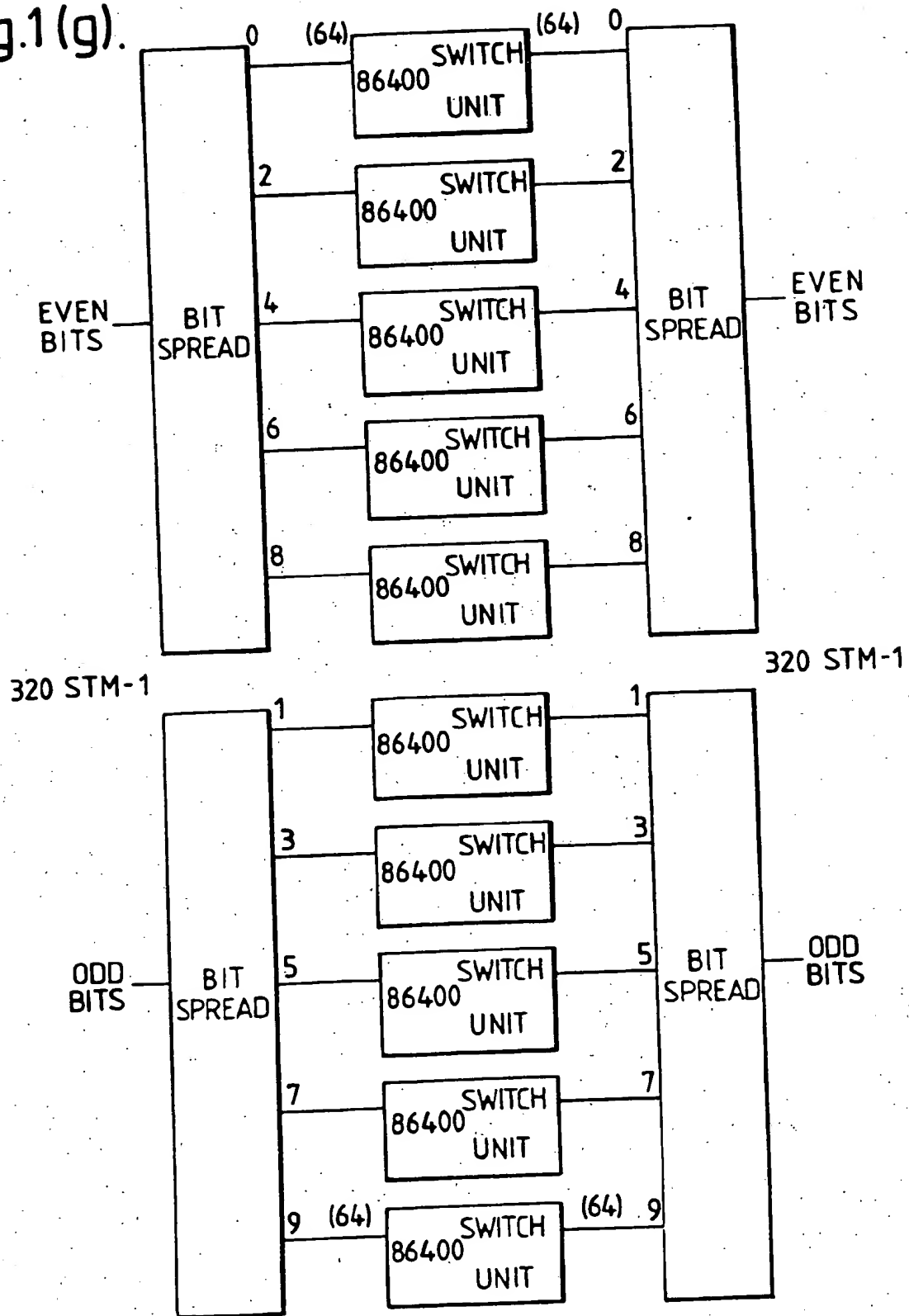


Fig.2(a&d).

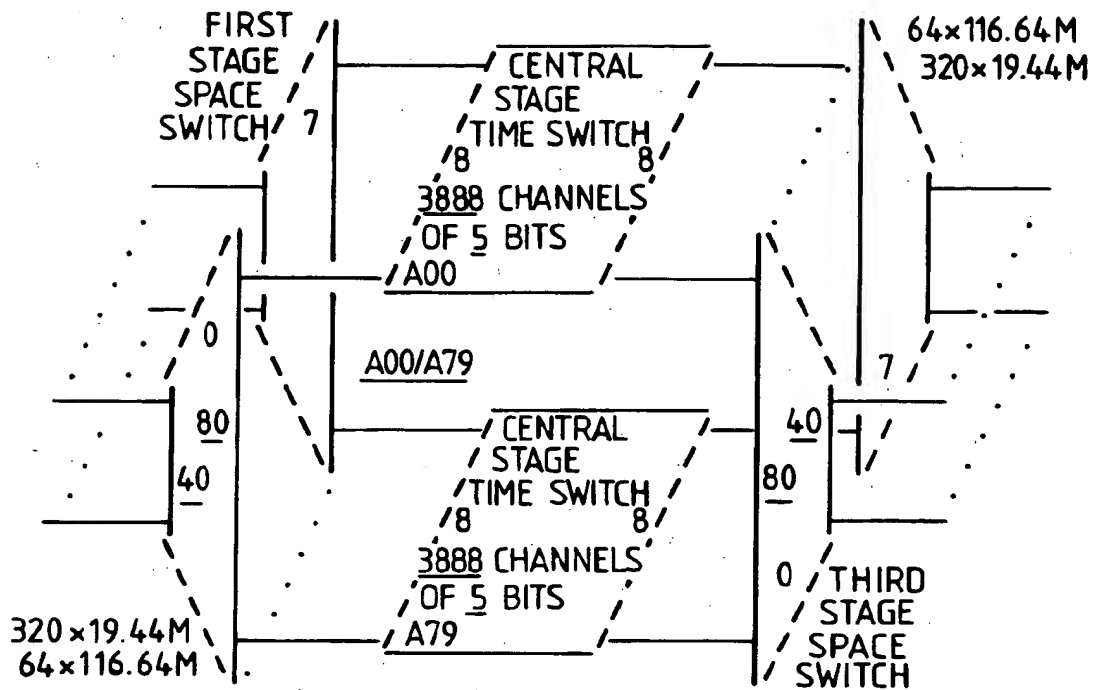


Fig 2(b).

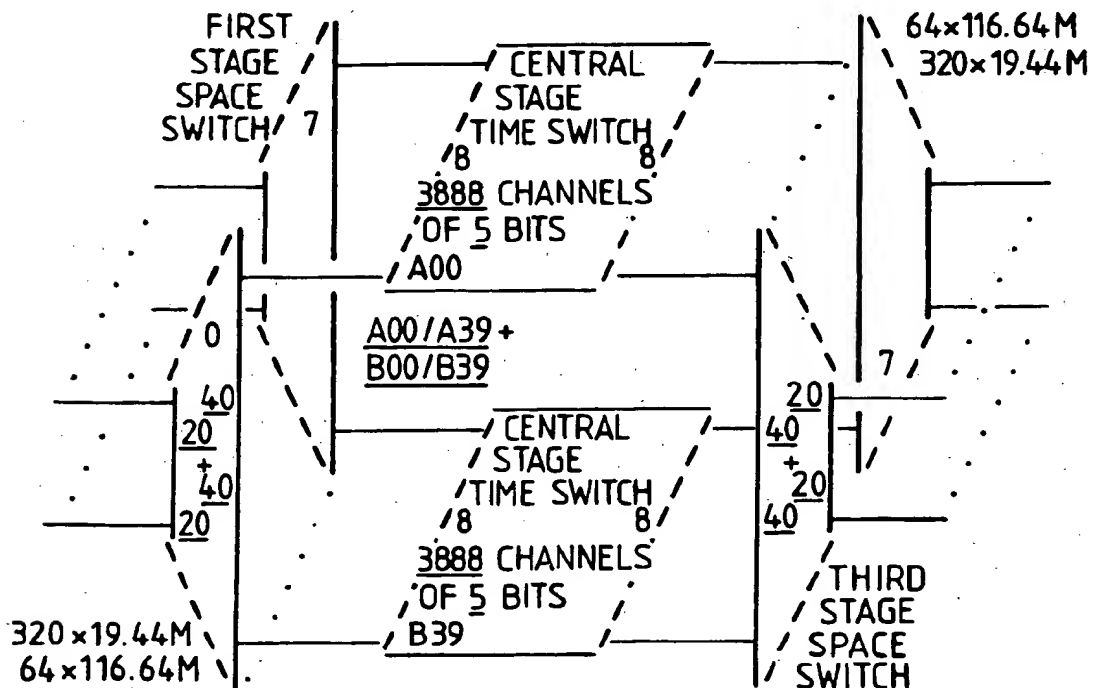


Fig. 2(c).

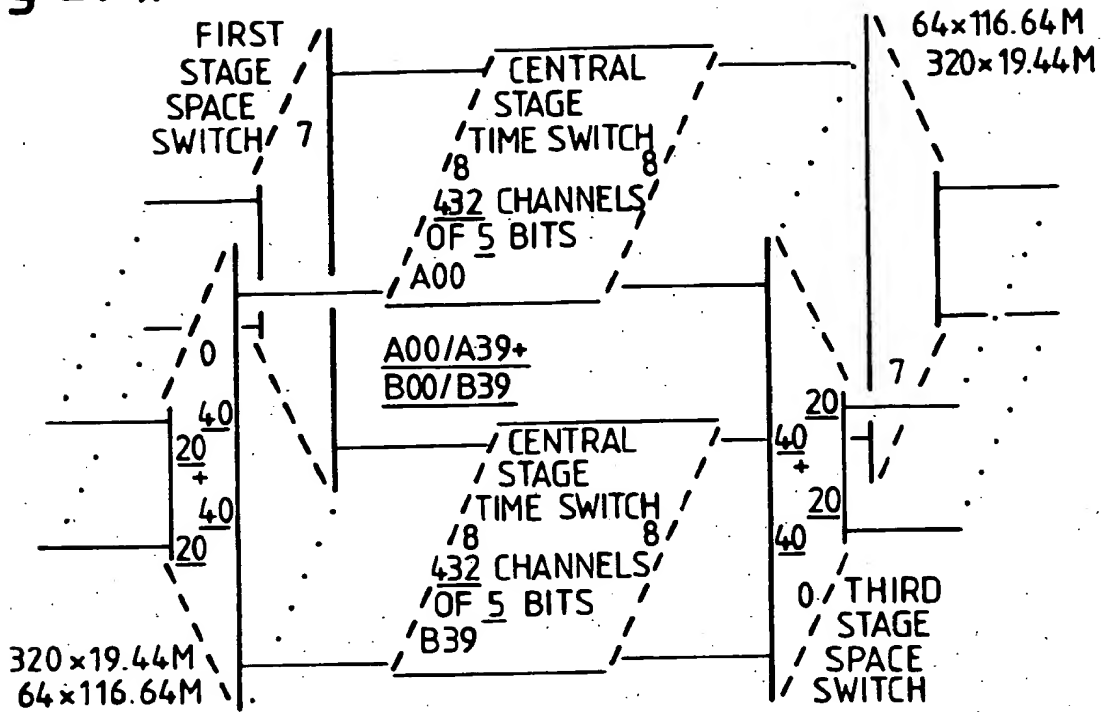


Fig. 2(e).

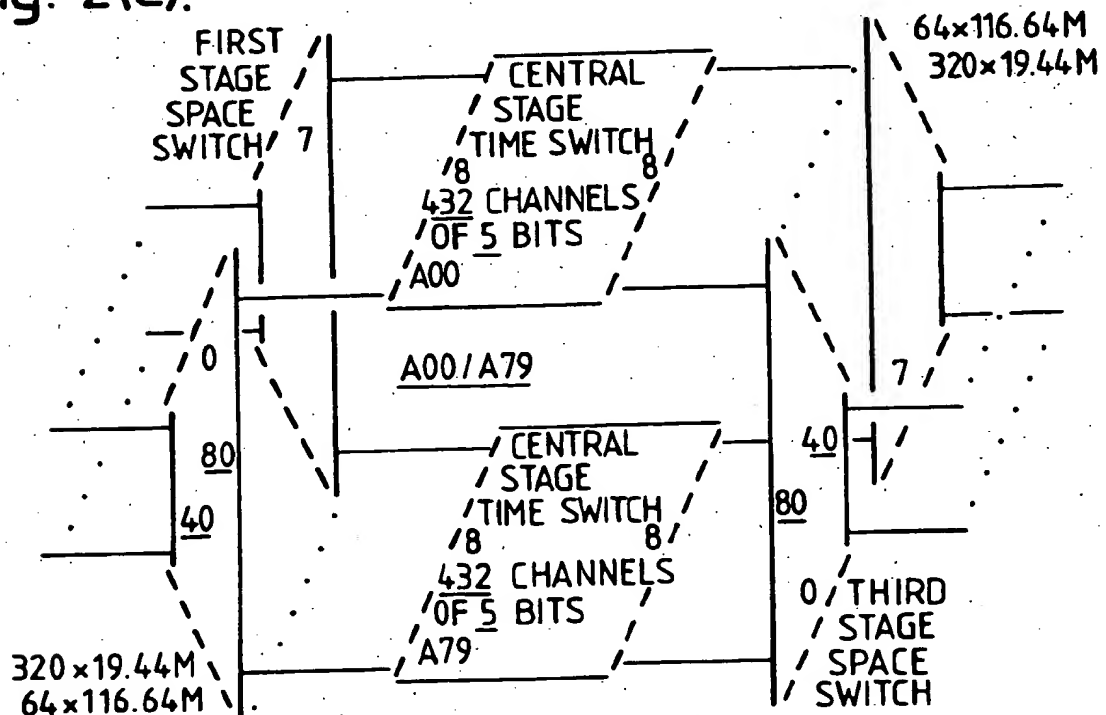


Fig. 2 (f).

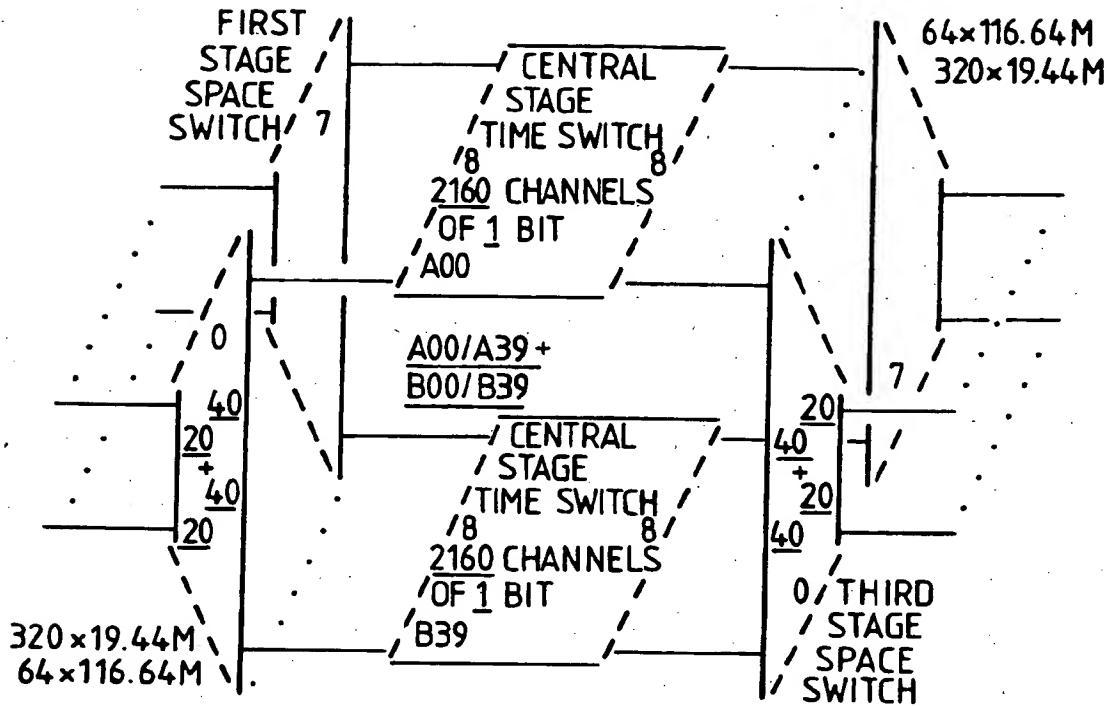


Fig. 2(g).

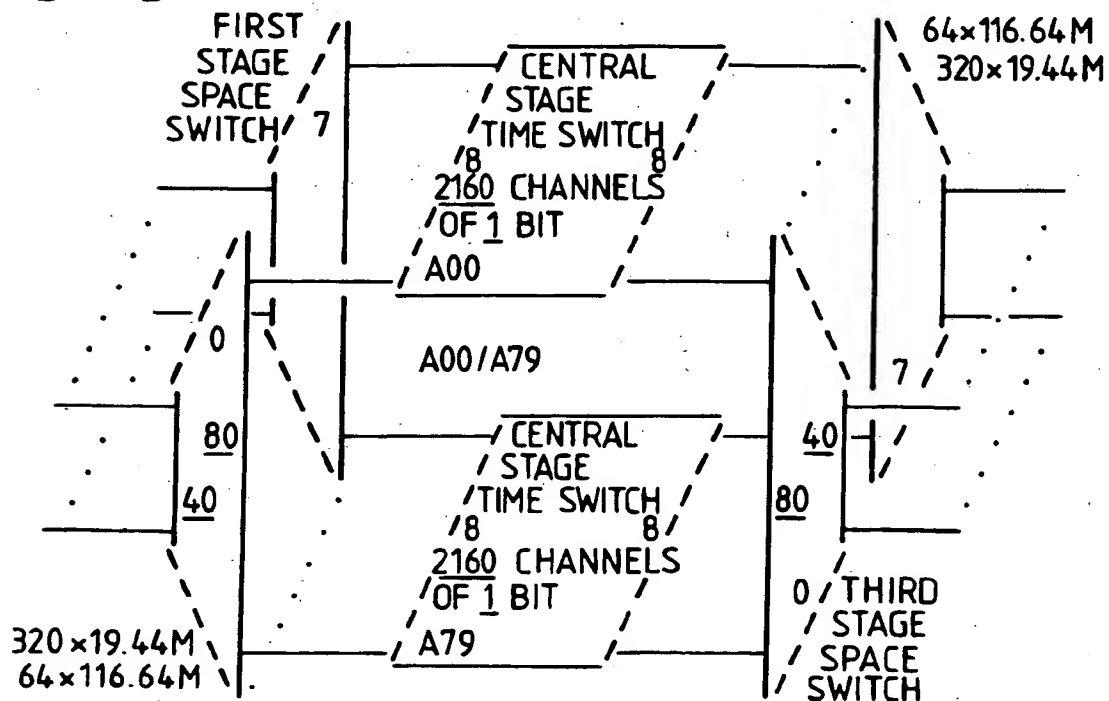


Fig.3.

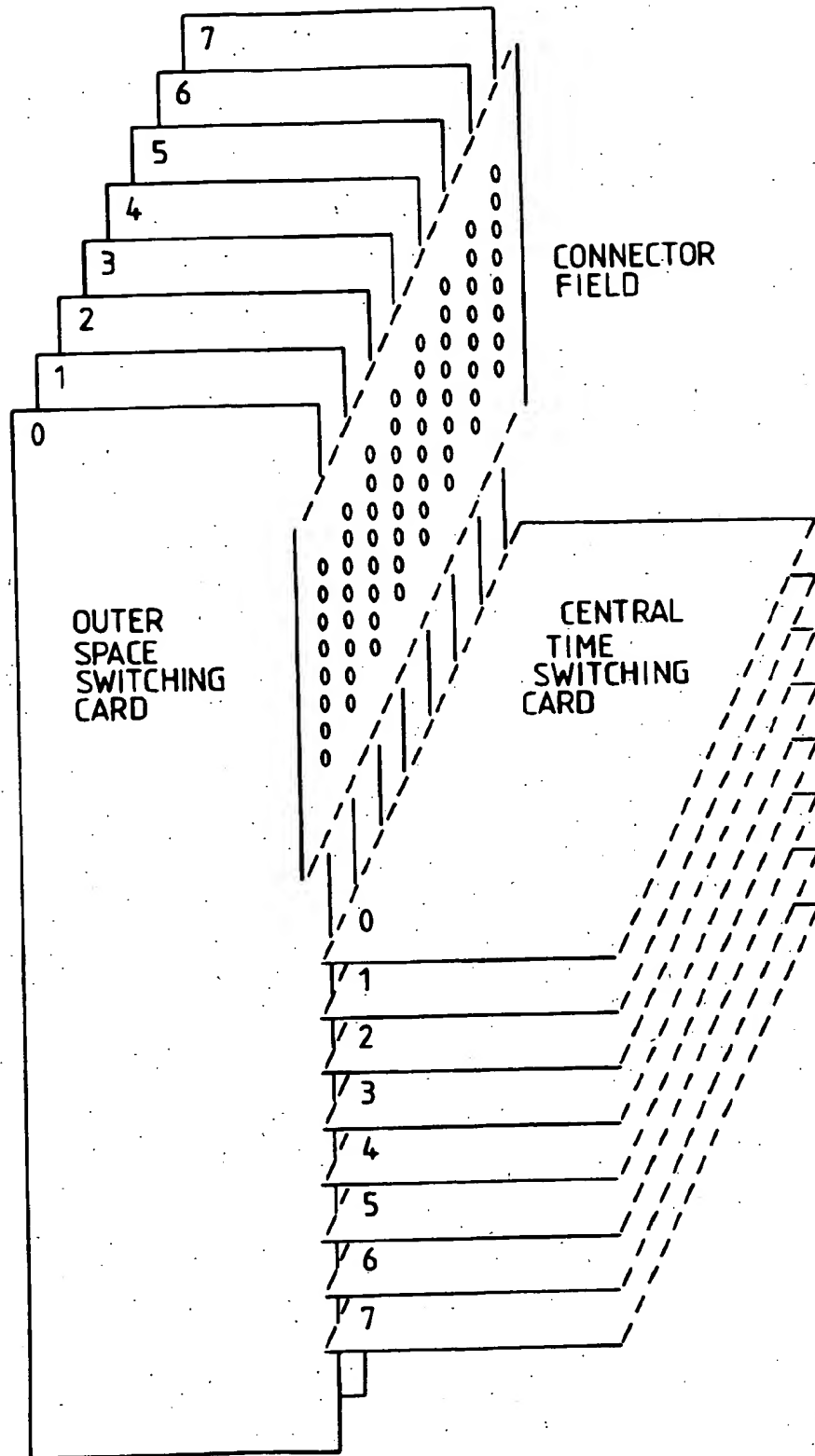


Fig. 4(a).

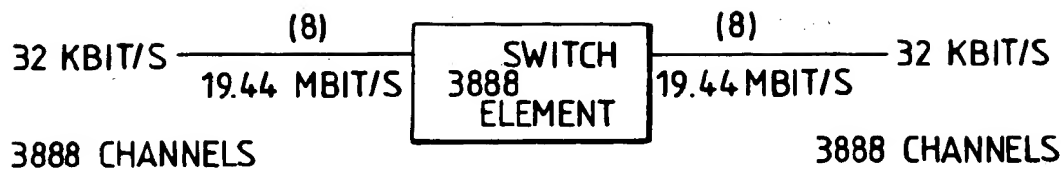


Fig. 4(b).

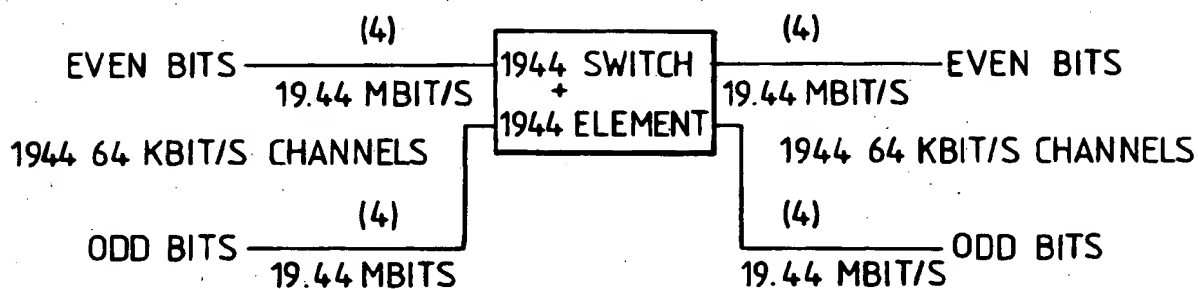


Fig. 4(c).

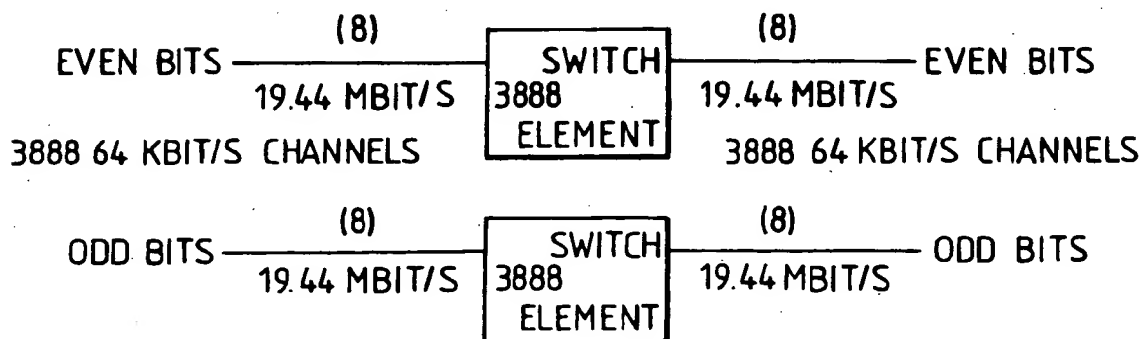




Fig. 4 (d).

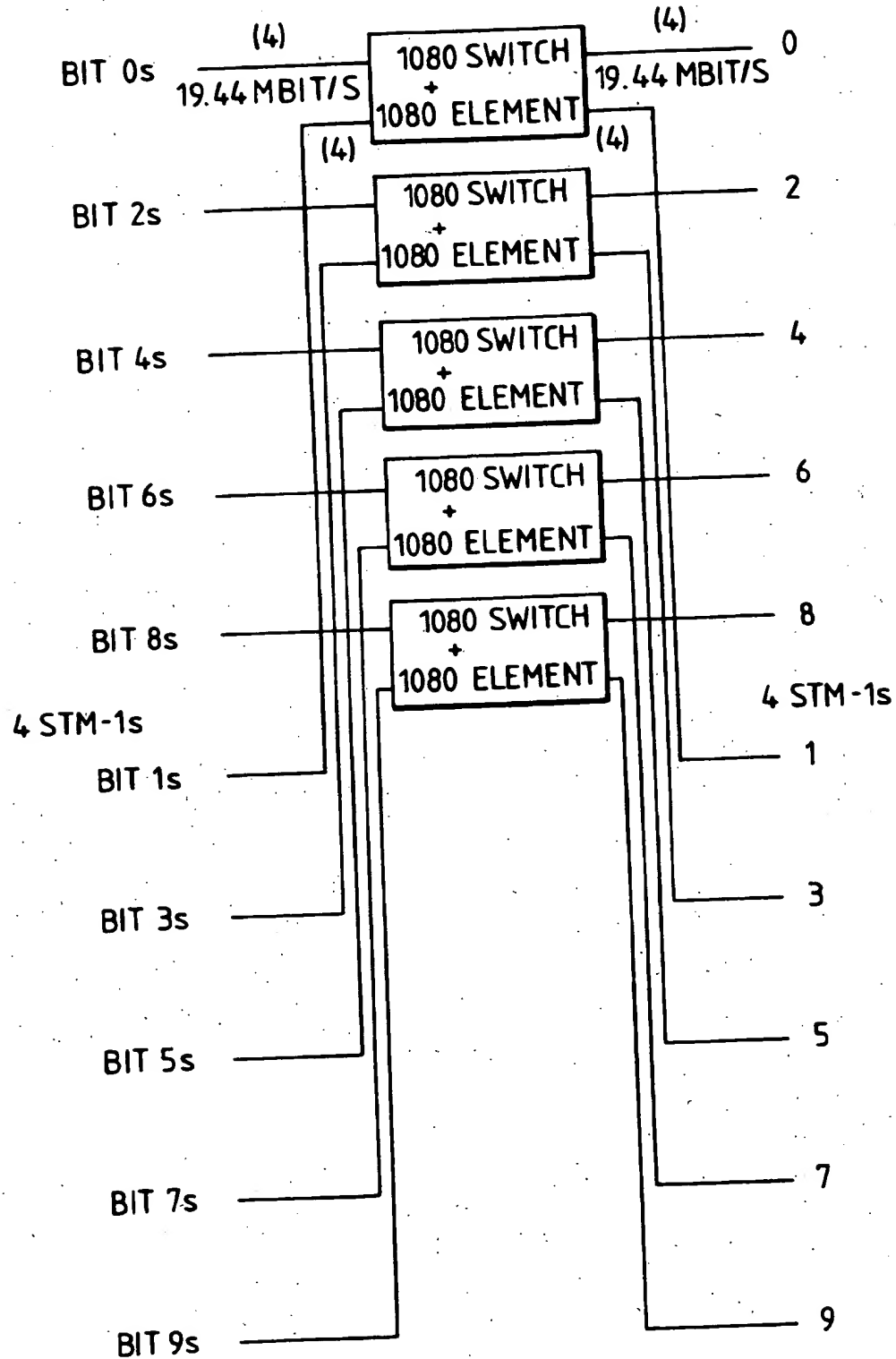


Fig. 4(e).

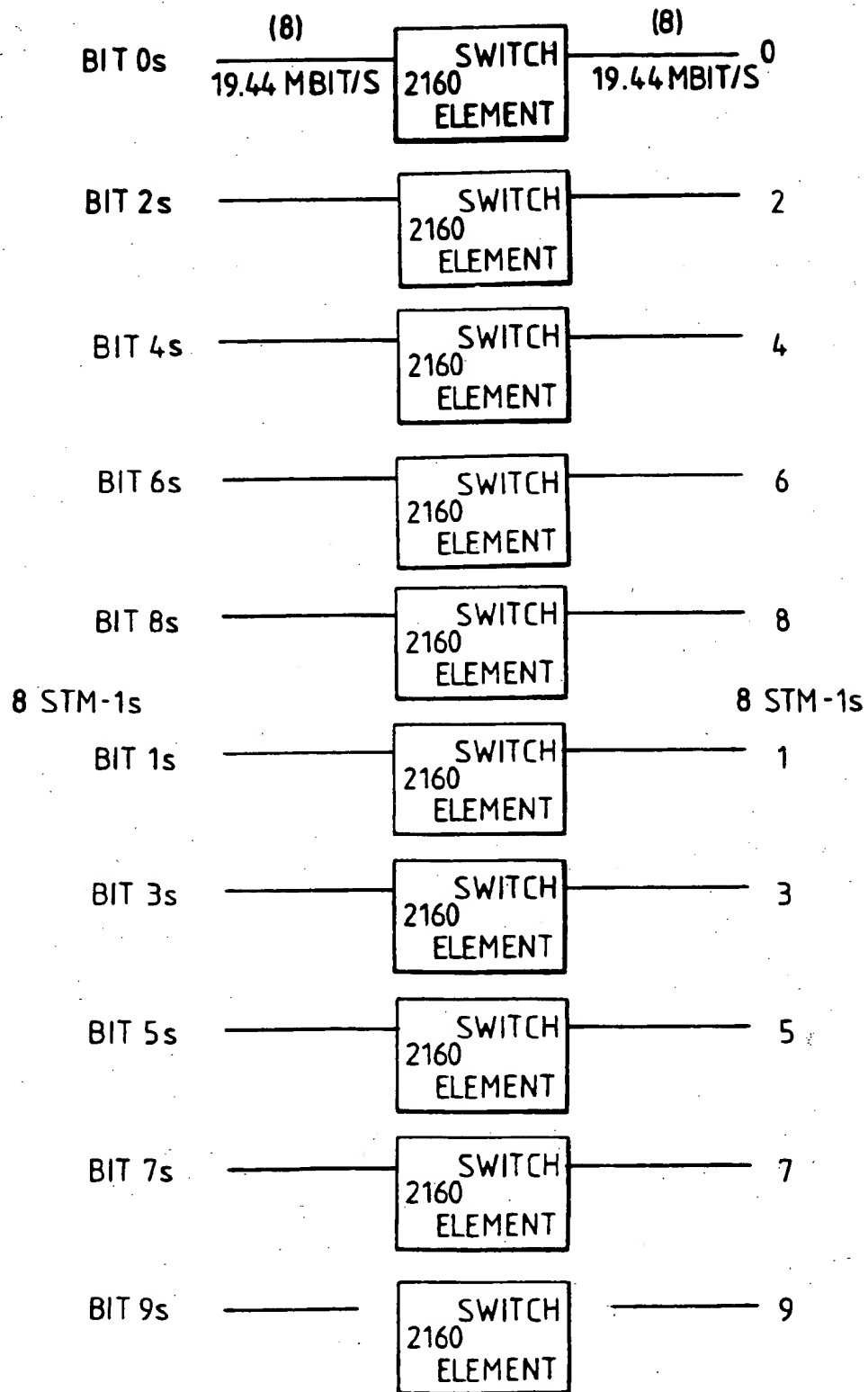


Fig.5(a).

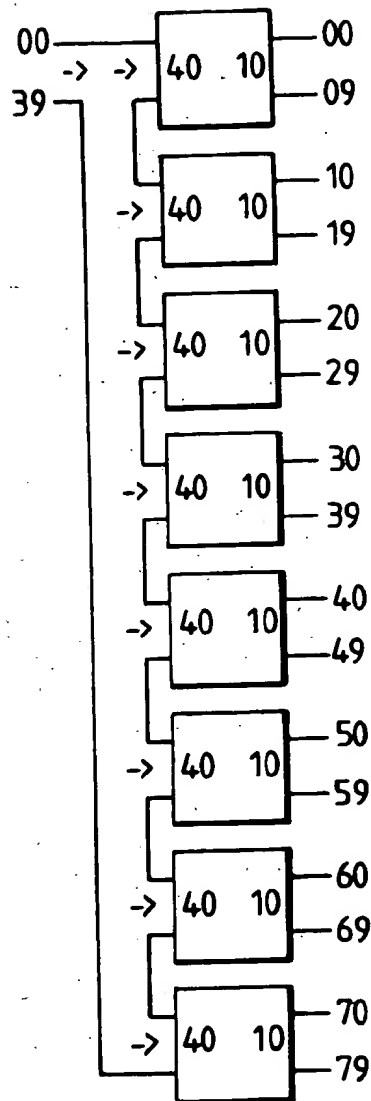


Fig.5 (b).

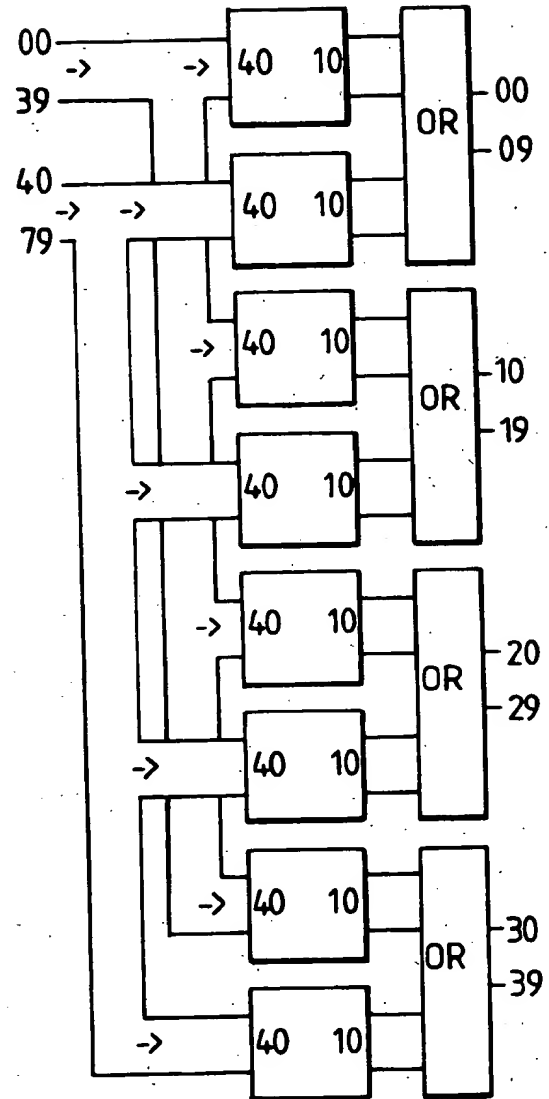


Fig.5(c).

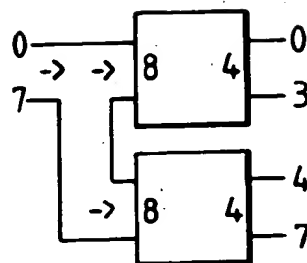


Fig. 6(a).

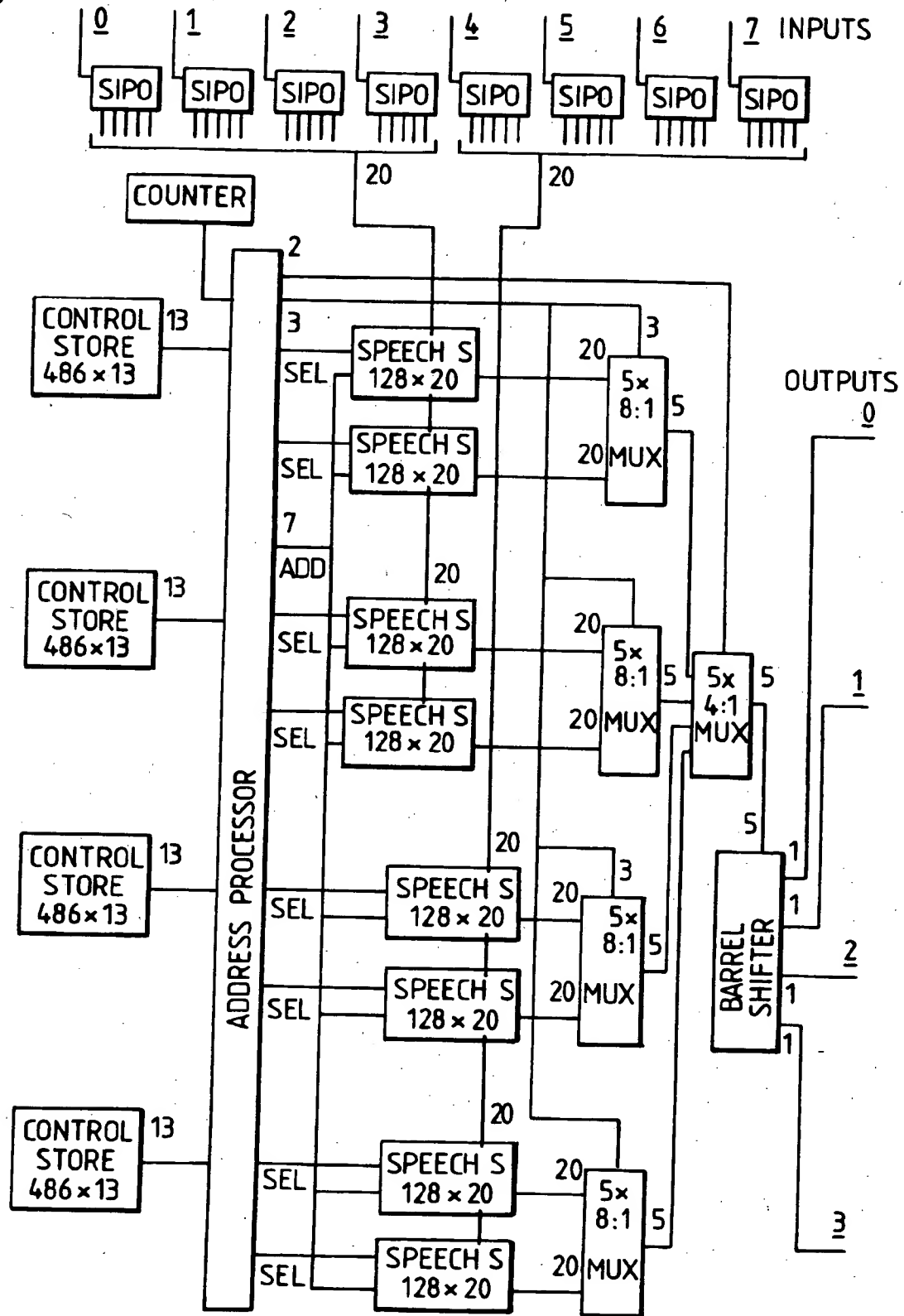


Fig. 6(b).

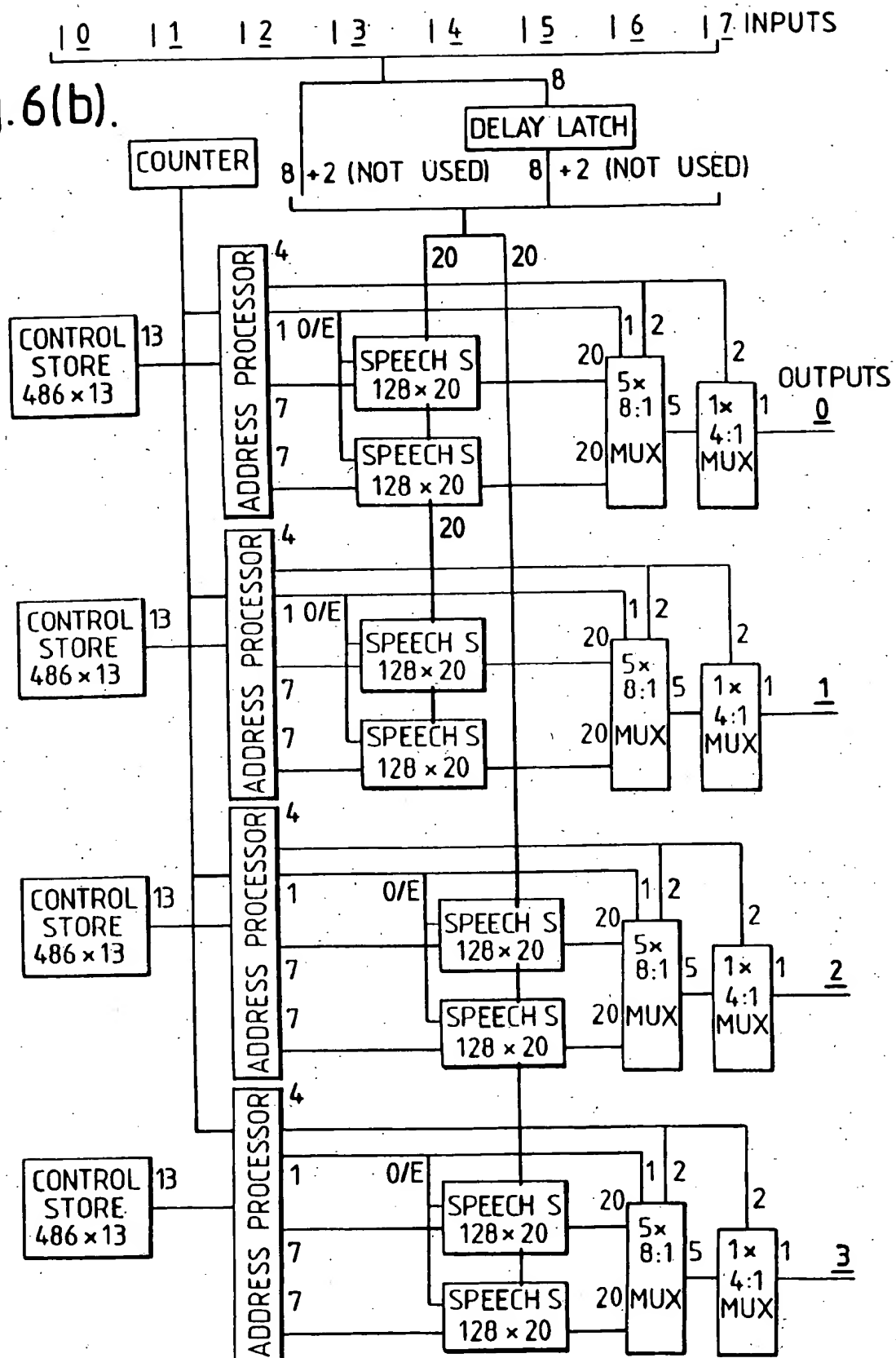


Fig.7.

INTERFACES	UNITS PER PLANE	AVAILABLE GRANULARITIES							
		VC 4	VC 3	VC 2	VC 12	VC 11	NX64 kb/s	64 kb/s	32 kb/s
4 (9k)	1 CARD	★	★	★	★	★	★	★	★
8 (19k)	1 CARD	★	★	★	★	★	★	★	★
16 (38k)	2 CARDS	★	★	★	★	★	★	★	★
32 (77k)	1 UNIT	★	★	★	★	★	★	★	★
64 (155k)	2 UNITS	★	★	★	★	★	★	★	★
160	5 UNITS + B/SPREAD	★	★	★	★	★	★	★	
320	10 UNITS + B/SPREAD	★	★	★	★	★			